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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application
Inventor(s): Krivokapic, et al.
SC/Serial No.: 09/711,445
Confirm. No.: 7218
Filed: November 13, 2000
Title: SELF-ALIGNED TRIPLE GATE SILICON-ON-INSULATOR (SOI) DEVICE

PATENT APPLICATION

Art Unit: 2811
Examiner: Owens, Douglas W.

**Customer No. 23910**

**CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8**

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on March 3, 2003.

(Attorney Signature)
Stephen R. Bachmann, Reg. No. 50,806
Signature Date: March 3, 2003



## RESPONSE C TO OFFICE ACTION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, DC 20231

Sir:

This RESPONSE C is in reply to the Office action mailed December 3, 2002. An appropriate Petition for Extension of Time to Respond is submitted herewith, together with the appropriate fee.

### Amendments

All amendments made herein comply with the format proposed by the revision to 37 CFR 1.121 (Manner of Making Amendments). Please amend the above-identified application as follows:



Attorney Docket No.: AMDI8399us0
//sbachmann/wp/amdi/8399/8399us0.013.respC.doc

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03/03/03-14:00

In the Title:

Please replace the title with the new title shown below:

**METHOD OF MAKING A DUAL GATE TRANSISTOR**

In the Drawings:

Enclosed are formal drawing replacement sheets for Figs. 1, 4B, 5B, 13A, 14A-C, 15A-C, and 16A, which include Applicant's desired changes, without markings, and comply with § 1.84. Subject to the approval of the Examiner, it is respectfully requested that the new drawing sheets be substituted for the originally filed drawing sheets for Figs. 1, 4B, 5B, 13A, 14A-C, 15A-C, and 16A. The changes are explained in the Remarks section of the present Response.